THERMAL DEVICES INTEGRATED WITH THERMOELECTRIC MODULES WITH APPLICATIONS TO CPU COOLING

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ABSTRACT
Over the past few years, the air cooling technology improvements present diminishing returns for microprocessors cooling applications. Presently most of the proposed future cooling technologies (i.e. pumped liquid cooling or vapor compressor refrigeration) may need some fluid moving device and a large remote heat exchanger which requires additional volume. Due to the complexity, reliability issues and space requirements it is preferred to extend the air cooling within the current form factors and using passive devices. This paper will show that optimized thermoelectric modules combined with two-phase (liquid/vapor) passive devices can further improve the cooling capability compared to conventional air cooling technologies at reasonable thermoelectric cooler (TEC) power consumption. Current computational fluid dynamics programs are not yet well equipped to find out the most optimized TEC geometry (for a given COP and given thermal requirements) in a reasonable amount of computation time. Therefore, two modeling steps are proposed: find out the preliminary TEC geometry using an 1D analytical program (based on uniform heat flux and a given COP) and use it as an input to CFD programs (i.e. Icepak®) for detailed predictions. Using this model, we confirmed that the conventional TEC technology must use some spreading device to dissipate the CPU heat to the TEC cold side. Different spreading devices are considered: solid metal, heat pipe, vapor chambers and single/two phase pumped cooling. Their individual performance integrated with TEC will be presented. In addition, we propose that the TEC performance to be controlled as a function of instantaneous CPU power consumption, ambient temperature and other parameters. This controller offers extra flexibility which can be used for either noise reduction or TEC power reduction. However, such power cycling of the TEC may affect the TEC reliability. Power cycling accelerated test data (>500,000 accelerated cycles) have been performed together with the life predictions will be presented in the paper.

Nomenclature

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
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<tbody>
<tr>
<td>1U</td>
<td>1U server size heat sink</td>
</tr>
<tr>
<td>A</td>
<td>Area [m²]</td>
</tr>
<tr>
<td>COP</td>
<td>coefficient of thermal performance</td>
</tr>
<tr>
<td>Dp</td>
<td>Pressure drop [Pa]</td>
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<tr>
<td>Fs</td>
<td>TEC Density factor defined as the ratio between the TEC element size and the gap between two adjacent TEC elements</td>
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<tr>
<td>hₐrea</td>
<td>equivalent heat transfer coefficient of the fins based on heat sink base area [W/m²°C]</td>
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<tr>
<td>HS</td>
<td>Heat sink</td>
</tr>
<tr>
<td>HX</td>
<td>remote heat exchanger</td>
</tr>
<tr>
<td>L</td>
<td>length of the heat sink [m]</td>
</tr>
<tr>
<td>ṁ</td>
<td>mass flow rate (kg/s)</td>
</tr>
<tr>
<td>P or Q</td>
<td>Power [W]</td>
</tr>
<tr>
<td>q</td>
<td>heat flux [W/m²]</td>
</tr>
<tr>
<td>SM</td>
<td>Solid metal base heat sink</td>
</tr>
<tr>
<td>T</td>
<td>temperature [°C]</td>
</tr>
<tr>
<td>TDP</td>
<td>Thermal design power [W]</td>
</tr>
<tr>
<td>TEC</td>
<td>Thermoelectric device</td>
</tr>
<tr>
<td>TIM</td>
<td>Thermal Interface Material</td>
</tr>
<tr>
<td>U</td>
<td>TEC Voltage [V]</td>
</tr>
<tr>
<td>W</td>
<td>width of the heat sink [m]</td>
</tr>
<tr>
<td>ZT</td>
<td>“Dimensionless” Figure of Merit for the Thermoelectric Material</td>
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Greek symbols

<table>
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<tr>
<th>Symbol</th>
<th>Description</th>
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<tr>
<td>θₓᵧ</td>
<td>thermal resistance [°C/W] between point x and y at uniform heat flux</td>
</tr>
<tr>
<td>ψₓᵧ</td>
<td>thermal resistance [°C/W] between point x and y at non-uniform heat flux</td>
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η fin efficiency

Subscripts
a ambient
c case temperature
cold, side cold side of the TEC
cond condenser
evap evaporator
fin fins
Fins Heat Sink fins
hot, side hot side of the TEC
in liquid in
j junction
max maximum
out liquid out
s sink

Introduction

The current air cooling technology improvements present diminishing returns for microprocessors cooling applications. It is well known that thermoelectric devices can provide some temperature drop equivalent to a refrigeration effect. Compared to pumped liquid cooling or vapor compression refrigeration the TEC have the advantage of having no moving parts and that occupies low volume. Due to complexity, reliability issues and space requirements it is preferred to extend the air cooling within the current form factors by using TEC devices.

Figure 1. Schematic of a Thermoelectric device

The thermoelectric technology (Fig. 1) is based on the well known Peltier effect. Peltier had shown that when an electrical current passes through the junction of two different types of conductors it results in a temperature change. As this effect can be used for refrigeration, TECs are also referred as solid state refrigeration devices. The TEC have already been proven in the telecommunications industry and several previous attempts [1-2] to propose TEC for microprocessor cooling have shown that for some boundary conditions they are not effective mainly due to high heat flux densities at the cold side or a high hot side thermal resistance. Previous applications created the industry misperception that TECs have always very low coefficient of performances (COP<1) could have been one major obstacle for past TEC implementation. Although true depending on the configuration and if vapor compression refrigeration performance is desired, COP greater than 3 is possible when applied with optimized configurations and specific boundary conditions. It can be guessed that the possible operation below ambient can generate some condensate in high humidity air, however an active feedback controller may prevent condensation and in the same time ensure the microprocessor cooling performance. Due to some expected CPU power cycling, TEC reliability may be of some concern. However this paper proposes to use TECs for only 30-40% improvements over air cooling within same form factor. In this case, the maximum ΔT(T\text{hot}-T\text{cold}) across TEC may be lower than 15 °C in the worst case which is much lower than the maximum allowable temperature difference for the TEC.

Figure 2. Integration of TEC with a spreading device

Figure 2 shows the proposed configuration for a TEC based device to be used in electronics cooling. The proposed cooling systems is an apparatus which includes a spreading device (copper block, vapor chamber, heat pipe, thermosiphon, or cold plate) used for uniform heat spreading to the cold side of the TEC. One or several TEC modules are used to introduce a negative resistance into the integration chain, thus decreasing the operating temperature of the spreading device. A heat sink/remote heat exchanger/cold plate is attached to the hot side of the TEC to dissipate the CPU heat and the TEC heat to the ambient air.
Figure 3. Simplified 1-D Thermal Resistance Chain

Figure 3 shows the simplified 1-D chain of thermal resistances. It can be seen that the TEC introduces a negative temperature drop into the chain. However the penalty is that more heat is introduced into the system due to the TEC power consumption. The heat flow is from the CPU to the ambient air (bottom to top in Fig. 3). However, across the TEC, the heat flow is from the low temperature side \( T_{\text{cold}} \) to the higher temperature side \( T_{\text{hot}} \). From a thermal resistance network point of view, the heat flow against the temperature gradient can be considered to be effectively a negative thermal resistance. Of course, this is not free as it requires some power input into TEC. It can be seen the effect of a negative temperature gradient across the components may ultimately reduce the CPU case temperature. The designer needs to mainly answer to what will be the power consumption of the TEC and what kind of heat sink should be used to achieve the specifications. There is a need to determine the feasibility of these concepts especially if the use of TECs can further extend air cooling and what are the trade offs to be made for the implementation of these concepts. This paper presents the key concepts regarding a TEC based solution addressing the capability, TEC power requirements for typical operating conditions, possible acoustic advantages associated with it and some limited reliability data. Reasonable constraints encountered in microprocessor cooling are taken into consideration.

**Metrics and Definitions**

Figure 4 shows the CPU with lidded package and a TEC based heat sink to be used for cooling of such package. The data presented in this paper is using this test vehicle to measure the performance of the TEC based cooling devices.

The most common metric used to compare the thermal performance of heat sinks is the sink to ambient thermal resistance defined as:

\[
\theta_{sa} = \frac{T_a - T_s}{Q_{CPU}} \tag{1}
\]

The thermal resistance of the spreader, whether it is a solid metal spreader, a vapor chamber, or a heat pipe, can be expressed as:

\[
\theta_{\text{TS/VCHP}} = \frac{T_s - T_{\text{cond,av}}}{Q_{CPU}} \tag{2}
\]

where \( T_{\text{cond,av}} \) is the average temperature over the top side of the spreader (thermosyphon/ vapor chamber/ heat pipe spreader/ copper plate).

The heat transfer coefficient is given by equation (3):

\[
h_{\text{area}} = \frac{1}{\theta_{\text{fin,eff}} \times A_{\text{base}}} \tag{3}
\]

One measure of performance of a TEC is the COP (coefficient of performance). It is the ratio of two heat flow terms as give by equation (4):

\[
\text{COP} = \frac{Q_{CPU}}{P_{\text{TEC}}} \tag{4}
\]

In other words, the COP is simply the amount of energy pumped for each Watt of power input to the TEC and its definition is identical to the definition of COP of a refrigeration system. Higher values of the COP means that less input power is required to move a given heat flow across the unfavorable temperature gradient. For example, a COP of 3 means that the electrical input power to the TEC is just 1/3 W for each 1.0 W moved from the cold side to the hot side.

**TEC Building Block**

**Heat Pipe integrated with the TEC**

Figure 5 shows a heat pipe based TEC concept proposed for cooling lower form factors where a larger remote heat sink can be accommodated. Here the spreading device is using a combination of 5 – 6 mm round grooved heat pipes embedded into some copper blocks. TECs are inserted between the heat sink (80 mm x 120 mm x 40 mm in size) and the heat pipes. This design can fit, for example, in some particular 1U server.

Figure 6 presents the statistical experimental data of the
concept presented in Figure 4. It can be seen that the sink to ambient resistance of about 0.1 C/W or less can be obtained for this particular design.

Figure 5. Heat pipe integrated with TEC prototype

![Heat pipe integrated with TEC prototype](image)

Figure 6. Test data for 20 samples using commercially optimized TECs at $Q_{CPU}=120$ W and COP=3

![Test data for 20 samples using commercially optimized TECs](image)

Figure 7. Thermal Capability for TEC with remote cooling using heat pipes for lidded package using a heat sink of 80x120x27 mm$^3$ with 0.3 mm thick fins spaced 1.3 mm apart; $T_{amb}=23^\circ$C, $\theta_{hp}=0.1^\circ$C/W, thermal grease of $R_{TIM}=0.4$ °Ccm$^2$/W. 20 sample data, tested at 120W with COP=3.

![Figure 7. Thermal Capability for TEC with remote cooling using heat pipes for lidded package using a heat sink of 80x120x27 mm$^3$ with 0.3 mm thick fins spaced 1.3 mm apart; $T_{amb}=23^\circ$C, $\theta_{hp}=0.1^\circ$C/W, thermal grease of $R_{TIM}=0.4$ °Ccm$^2$/W. 20 sample data, tested at 120W with COP=3.](image)

Figure 8. Thermal Capability for TEC with thermosiphon

Figure 8 and Figure 9 shows the thermal capability for different spreading devices (thermosiphon or solid copper). The thermosiphon is used to spread the heat to a larger heat exchanger (80 mm x 80 mm x 40 mm) but the solid metal only to a smaller one (80 mm x 80 mm x 20 mm). In Fig. 9, it can be seen that the improvement are significant at lower powers but below COP of 3 it is not reasonable to cool more that 108 W. The key message is that there is a threshold where solid metal TEC is efficient for lower TDPs but is insufficient for larger powers. Due to this fact we recommend using the TEC and solid metal for larger form factors and heat pipe remote based TECs for all form factors.

A 3d model using the commercial software ICEPAK® has been performed. Figure 10 (a) and 10(b) shows the cold side and respectively hot side TECs temperature profiles, in case when a thermosiphon is used as a spreading device. It can be seen that
the non-uniformity is in excess of 8 °C for both cold and hot side and that the profile at the cold side is much different compared to the hot side. This is mainly due to non-uniform air temperature across the fins and the non uniform spreading through the spreading devices. The key message from this figure is that this non-uniformity is significant and should be taken into account when a detailed design is done.

Figure 9. Thermal Capability for TEC with solid metal base

(a) TEC Cold Side    (b) TEC Hot Side

Figure 10. Temperature profile on the TEC cold and hot side (thermosiphon situation)

Figure 11 shows the performance for TEC based devices. It can be seen that the effective heat transfer coefficient (htec) on the top surface of the base of the heat sink plays a significant role in the performance improvements due to TEC. For low effective heat transfer coefficients the TEC is not so effective, while at higher values the performance can significantly improve compared to traditional non-TEC air cooling. The performance of the TEC is also dependent on the thermal resistance of both TIM A and TIM B materials, although the TIM on the hot side plays a larger role (heat flow through TIM B is larger than the heat flow through TIM A).

Figure 11. The influence of the hot side resistance

Figure 12. Solution Domain Example for TEC Manufacturing Optimization

Figure 12 shows the solution domain optimization for a TEC geometry. The graph shows that for the same thermal performance (Ψsa=0.15 °C/W ; TDP=120 W and COP=3) one can find a infinite number of TEC geometries & voltage combinations. It is up to the TEC manufacturer to choose the most cost effective TEC from this wide geometry options, but it is preferred that the voltage to be below 12 V so the existing power supplies can be used.

Figure 13 shows the TEC power consumption as a function of the CPU power dissipation. In this particular example, the case to ambient resistance is kept constant, which potentially may improve the CPU reliability. It can be seen that the TEC power consumption decreases significantly at lower CPU power levels. In other words, the TEC solution can be designed for the worst conditions but a majority of the users (let’s say users who use only 80% of TDP) will require to use much lower TEC powers when compared with the users who are operating at the worst conditions.
resistance is 0.13 °C/W. There is also a solution for the 8 V case first. At a COP of 4, the resulting thermal performance at both fan voltage levels (fan speed). The penalty graph shows that the designer can keep same thermal running at 8 V than when running at 12 V. However, this 60 x 60 mm fan was measured to be 0.8 BA lower when boundary conditions. For this study, the noise level of a Delta reduction by using the TEC based devices for some specific figures show that the designer has multiple choices in developing the algorithm for the TEC controller. As a basic recommendation the controller should address the thermal performance, noise reduction, TEC power consumption and preventing condensation.

Figure 13. TEC Power Consumption vs. CPU Power

Figure 14. Noise Reduction for TEC based solutions

Figure 15. Bivariate Fit of Mean Electrical Resistance by Number of Power Cycles

TEC Reliability Data

It is well know that the Tec reliability is mainly influenced by the power cycling and temperature drop across the hot side and cold side. Thermal fatigue resulting from temperature gradients across the TEC was identified as the primary failure mechanism. Power cycling at elevated temperature gradients (ΔT) was performed to accelerate this failure mechanism to predict reliability performance over time in the field. Most of the processor companies validates enabling component to a 7 year lifetime.

Thus:

\[ R(t, \Delta T) = \alpha + \beta (\Delta T)^N \]  

where \( \alpha \) is the electrical resistance at time 0 in Ω, \( N \) is the power law coefficient, \( t \) is the time (# of cycles), \( \beta \) is a constant coefficient, \( \Delta T \) is the temperature difference across TEC in °C. Linear regression was performed on the empirical data for resistance vs. time to extract the model parameters. The resulting Fig. 16 is used to calculate the model parameters. Thus : \( N \) is calculated as 8.1; \( \ln(\beta) \) as -40.57 and \( \alpha \) as 0.893.

Defining the failure as a 10% increase in resistance, per TEC industry best known method, the TEC failure is predicted (using equation 5) to occur after 11 million cycles at a conservative 15C assumption for \( \Delta T_{use} \) (operating temperature gradient). For \( \Delta T_{use} \) of 12C, failure is predicted after 67 million cycles, and for \( \Delta T_{use} \) of 10C, failure is predicted after 295 million cycles. The overall reliability assessment via power cycling of these commercially available TEC components suggests that thermal fatigue is a highly accelerated failure mechanism and poses a low risk for early failures in the field.
Conclusions

This paper presents the thermal and reliability capability of TEC based cooling devices with application to Architecture II type CPU. By using different spreading devices substantial performance can be obtained compared to conventional air cooling. For example, for particular sets of reasonable boundary conditions, about 40% reduction in sink to ambient resistance may be obtained. In the majority of cases, it was found out that the TEC is exposed to non-uniform heat flux/temperature boundary conditions on both the cold side and hot side. Data from 20 samples shows that this model has good prediction accuracy (less than 10% error). Design of Experiments (DOEs) shows that the sink to ambient thermal resistance can be improved by more than 40%-60% if TECs are optimized over a range of reasonable boundary conditions (the target Coefficient of Performance (COP) was chosen to be COP=3 for most of the cases). Test data from 20 samples have shown a sink to ambient thermal resistance of 0.11 °C/W for a CPU power of 120 W. This cooling performance is comparable with refrigeration type performance. A knowledge based approach was taken in assessing the reliability of commercially available ceramic based TECs with the prediction of more than 11 million cycles at a conservative 15C assumption for ΔTuse (operating temperature gradient) and for ΔTuse of 12C, failure is predicted after 67 million cycles.

References
